



Chip Card & Security ICs

SLE 5552

Intelligent 256-Byte EEPROM
with Write and Read-Out Protection function
and Programmable Security Code

SLE 5552 Short Product Information		Ref.: SPI_SLE5552_0506.doc
Revision History: Current Version 2006-05-19		
Previous Releases:		
Page	Subjects (changes since last revision)	

Important: Further information is confidential and on request. Please contact:
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Information

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Warnings

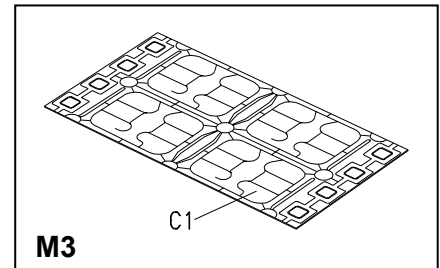
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Intelligent 256-Byte EEPROM with Write and Read-Out Protection Function and Programmable Security Code (PSC)

Features

- **Downward compatibility to SLE 4442 & SLE 5542**
- **256 x 8 bit EEPROM organization of Data Memory**
- **256 x 1 bit Protection Memory**
 - Byte-wise write protection of first 32 addresses (byte 0...31) of Data Memory
 - Manufacturer Code for unique identification of application
 - Byte-wise read-out protection last 224 addresses (byte 32...255) of Data Memory
- **Data Memory (addresses 0...255) alterable only after verification of 3-Byte Programmable Security Code (PSC)**
- **Read-protected Data Memory (addresses 32...255) readable only after verification of 3-Byte Programmable Security Code (PSC)**
- **Two-wire link protocol**
 - Byte-wise addressing
 - End of processing indicated at data output
- **Contact configuration and Answer-to-Reset (synchronous transmission) in accordance to standard ISO/IEC 7816**
- **Sophisticated electrical characteristics**
 - Ambient temperature $-40 \dots +80^{\circ}\text{C}$ for chip, $-25 \dots +80^{\circ}\text{C}$ for module
 - Supply voltage $5\text{ V} \pm 10\%$
 - Supply current $< 3\text{ mA}$ (typical $600\ \mu\text{A}$)
 - EEPROM erase / write time 5 ms
 - ESD protection typical $4,000\text{ V}$
 - EEPROM Endurance minimum $100,000$ erase / write cycles¹⁾
 - Data retention for minimum of 10 years ¹⁾
- **Advanced $1.2\ \mu\text{m}$ CMOS-technology optimised for security layout**
 - EEPROM-cells protected by shield
 - Shielding of deeper layers via metal
 - Sensory and logical security functions
 - No isolation on backside necessary



¹⁾ Values are temperature dependent.

1 Ordering and Packaging information

Table 1 Ordering Information

Type	Package ¹⁾	Remark	Ordering Code
SLE 5552 C	Die (on Wafer)	unsawn	on request
SLE 5552 D	Die (on Wafer)	sawn	on request
SLE 5552 M3	T-M3.2-6		on request
SLE 5552 MFC3	S-MFC3.1-6-1	FCoS™	on request

Pin Description

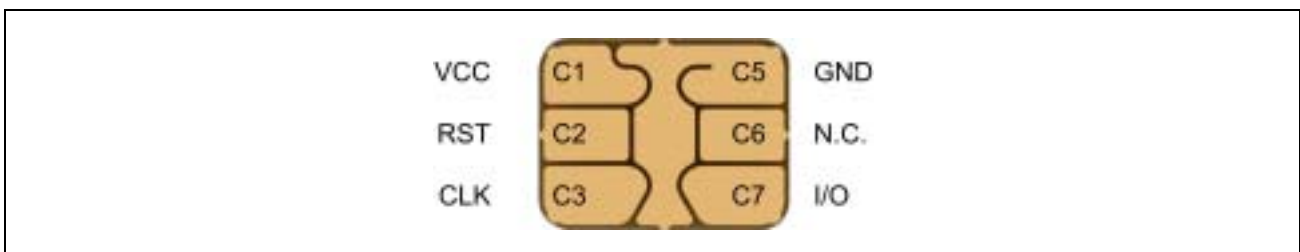


Figure 1 Pin Configuration Wire-bonded Module M3.2 (top view)

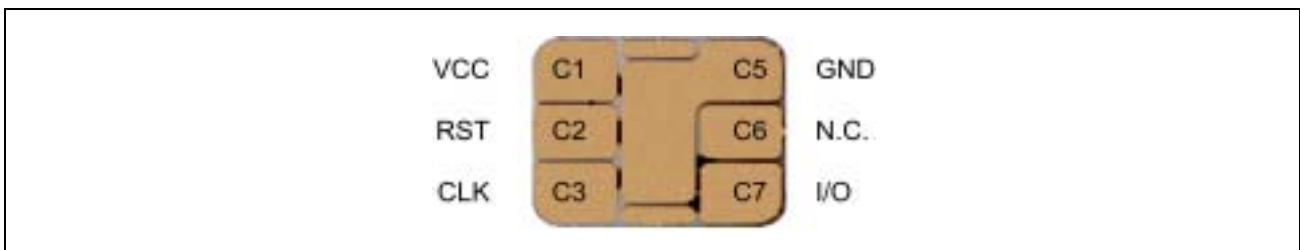
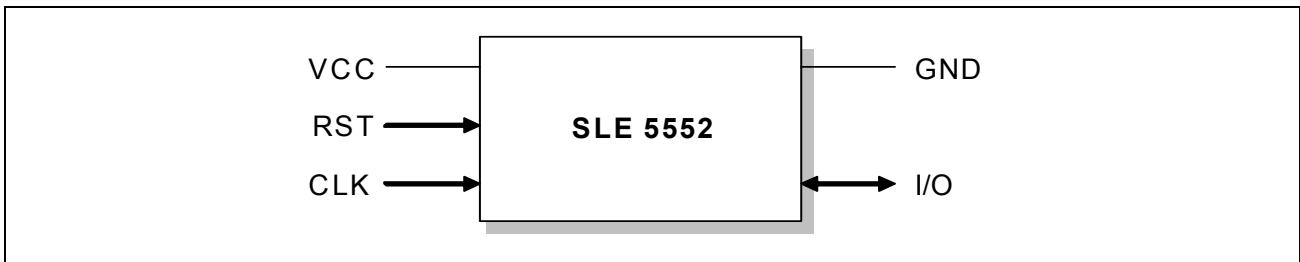


Figure 2 Pin Configuration Module Flip Chip MFC3.1 (top view)

¹⁾ Available as a Module Flip Chip (MFC3), wire-bonded module (M3) for embedding in plastic cards or as a die on unsawn (C) / sawn wafer (D) for customer packaging


Figure 3 Pad Configuration Die
Table 2 Pin Definitions and Functions

Card Contact	Symbol	Function
C1	VCC	Supply voltage
C2	RST	Control input (Reset Signal)
C3	CLK	Clock input
C5	GND	Ground
C6	N.C.	Not connected
C7	I/O	Bi-directional data line (open drain)

2 Circuit Description

Memory Organization

The memory is organized in a **Data Memory** of 256 byte.

Write and Read-Out Protection of Data Memory

- **Write Protection Flags:** Each of the first 32 bytes of the Data Memory can be irreversibly protected against data change by writing the corresponding bit in the **Protection Memory**. Dependent on the state of the protection bit the Data Memory is read only (ROM) or may be erased and written again (EEPROM). Change of the manufacturer code (Application ID and Chip Coding) is only possible by the chip manufacturer.
- **Read-Out Protection Flags:** Each of the last 224 bytes of the Data Memory can be irreversibly protected against read-out by writing the corresponding bit in the **Protection Memory**.

Programmable Security Code

- Change of data of the Data Memory (addresses 0...255) and write a bit of the Protection Memory is only possible after verification of the 3-Byte **Programmable Security Code (PSC)**.
- Read-out of read-protected Data Memory (addresses 32...255) only after verification of the 3-Byte **Programmable Security Code (PSC)**.

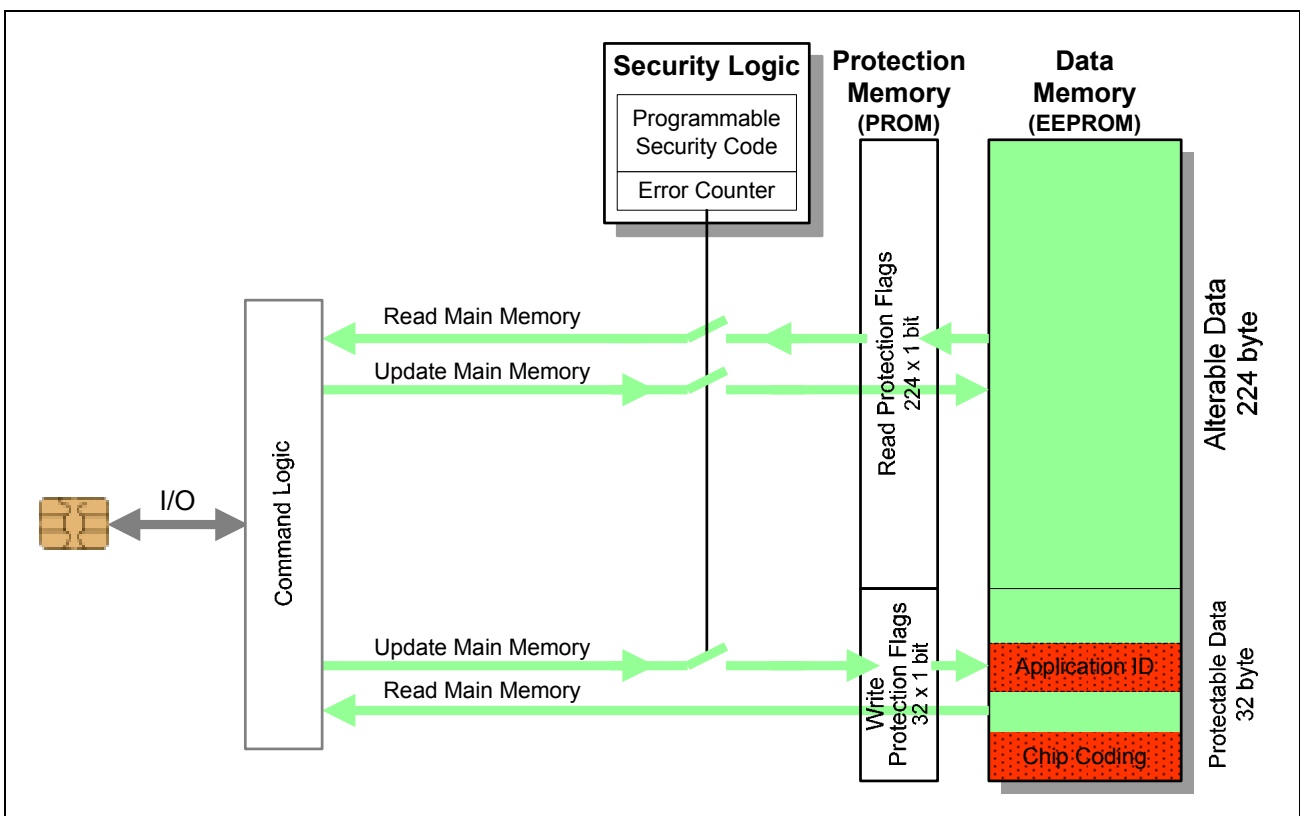


Figure 4 Memory Overview SLE 5552